Applicant respectfully submits that each of independent Claims 1 and 16, as amended herein, are not rendered obvious or unpatentable over any permissible combination of the teachings of Hshieh '678 and Luo and that each of the rejections should be withdrawn.

Dependent Claims 2-15 are believed to be clearly patentable for all of the reasons indicated above with respect to amended independent Claim 1, from which they depend, and even further distinguish over the cited references by reciting additional distinguishing limitations.

Since the Applicants have fully responded to each rejection set out in the Office Action, it is respectfully submitted that in regard to the above amendment and remarks that the pending application is patentable over the art of record and prompt review and issuance is accordingly requested. Should the Examiner be of the view that an interview would expedite consideration of this Amendment or of the application at large, request is made that the Examiner telephone the Applicants' undersigned attorney at (908) 518-7700 in order that any outstanding issues be resolved.

Respectfully submitted,

Karin L. Williams

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Certificate of Mail
I hereby certify that this document is being deposited with the US Postal Service as first class mail under 37 C.F.R. 1.8 and addressed to the Assistant Commissioner for Patents, Washington, DC 20231 on April 4, 2003

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Version with markings to show changes made

In The Claims

Claims 1 and 16 have been amended as follows.

1. (Amended) A trench MOSFET transistor device comprising:

a silicon substrate of a first conductivity type;

a silicon epitaxial layer of said first conductivity type over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

a trench extending into said epitaxial layer from an upper surface of said epitaxial layer;

an insulating layer lining at least a portion of said trench;

a conductive region within said trench adjacent said insulating layer;

a body region of a second conductivity type provided within an upper portion of said epitaxial layer and adjacent said trench;

a source region of said first conductivity type provided within an upper portion of said body region and adjacent said trench;

an upper region of second conductivity type within an upper portion of said body region and laterally adjacent said source region, wherein said upper region does not extend to said trench, and wherein said upper region [having] has a higher majority carrier concentration than said body region; and

a source contact region disposed on said epitaxial layer upper surface, said source contact region comprising: (a) a doped polycrystalline silicon contact region in electrical contact with said source region and (b) a metal contact region adjacent said doped polycrystalline silicon contact region and in electrical contact with said source region and with said upper region.

16. (Amended) A trench MOSFET transistor device comprising:

an N-type silicon substrate;

an N-type silicon epitaxial layer over said substrate, said epitaxial layer having a lower majority carrier concentration than said substrate;

a trench extending into said epitaxial layer from an upper surface of said epitaxial layer;

a silicon oxide insulating layer lining at least a portion of said trench;

a doped polycrystalline silicon conductive region within said trench adjacent said insulating layer;

a P-type body region provided within an upper portion of said epitaxial layer and adjacent said trench;

an N-type source region provided within an upper portion of said body region and adjacent said trench;

a P-type upper region within an upper portion of said body region and laterally adjacent said source region, wherein said upper region does not extend to said trench, and wherein said upper region [having] has a higher majority carrier concentration than said body region;

a borophosphosilicate glass insulating region disposed over said conductive region, said insulating region extending above said epitaxial layer upper surface; and

a source contact region disposed on said epitaxial layer upper surface and laterally adjacent said insulating region, said source contact region comprising: (a) a doped polycrystalline silicon contact region having N-type doping and (b) a metal contact region adjacent said doped polycrystalline silicon contact region and in electrical contact with said source region and with said upper region.